CLAIMS

1. A method for configuring an integrated device in a first processor comprising:

decoding a memory configuration access within a second processor, the second processor coupled to the first processor, to a configuration cycle;

routing the configuration cycle to a chipset based at least in part on a routing information; and

forwarding the configuration cycle.

2. The method of claim 1 wherein the configuration cycle is routed to the chipset via a network fabric.

3. The method of claim 1 wherein the network fabric is a plurality of point to point links.

4. The method of claim 1 wherein the chipset has a bridge and adheres to a PCI type interconnect that is either PCI or PCI Express.

5. The method of claim 2 wherein the second processor is coupled to the first processor via the network fabric.

6. A method for configuring an integrated device in a first processor comprising:

decoding an Input Output (IO) configuration access within a second processor, coupled to a first processor, to a configuration cycle; and

routing the configuration cycle to the integrated device based at least in part on a routing information.

7. The method of claim 6 wherein the configuration cycle is routed to the integrated device via a network fabric.

8. The method of claim 6 wherein the network fabric is a plurality of point to point links.

9. The method of claim 6 wherein the configuration adheres to a PCI type interconnect.

10. The method of claim 6 wherein the PCI type interconnect is either PCI or PCI Express.

11. The method of claim 7 wherein the second processor is coupled to the first processor via the network fabric.

12. A processor comprising:

a decoder to decode either a memory or IO configuration access to a configuration cycle; and

to transmit the configuration cycle to either a chipset or integrated device.

13. The processor of claim 12 wherein the transmission of configuration cycle to either a chipset or integrated device is via a PCI type interconnect that is either PCI or PCI Express.

14. The processor of claim 12 wherein the configuration cycle is routed to the integrated device or chipset via a network fabric.

15. A system comprising:

a first processor with an decoder coupled to a second network component with an integrated device,

the decoder to decode either a memory or IO configuration access to a configuration cycle; and

to transmit the configuration cycle to either a chipset or integrated device, wherein the configuration cycle adheres to a PCI type interconnect.

16. The system of claim 15 wherein the PCI type interconnect is either PCI or PCI Express.

17. The system of claim 15 wherein the configuration cycle is routed to the integrated device or chipset via a network fabric.

18. An article of manufacture comprising:

a machine-readable medium having a plurality of machine readable instructions, wherein when the instructions are executed by a system, the instructions provide to configure an integrated device in a processor or network component by:

decoding either a memory or IO configuration access to a configuration cycle; and

transmitting the configuration cycle to either a chipset or integrated device, wherein the configuration cycle adheres to a PCI type interconnect.

19. The article of manufacture of claim 18 wherein the chipset or integrated device is coupled to the decoder via a network fabric.

20. The article of manufacture of claim 18 wherein the PCI type interconnect is either PCI or PCI Express.

21. A method for configuring an integrated device in a first processor comprising:

decoding a memory configuration access within a second processor, the second processor coupled to the first processor, to a configuration cycle; and

routing the configuration cycle from a chipset to the first processor via a bridge.